1. (As Filed) A programmable wire structure for an integrated circuit, comprising:

a programmable switch coupling two nodes, said switch having a first state that connects said two nodes, and said switch having a second state that disconnects said two nodes; and

a configuration circuit coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and

a first metal layer fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer.

2. (As Filed) The structure of claim 1, wherein a second metal layer is fabricated substantially above said switch and said configuration circuit.

3. (As Filed) The structure of claim 1, wherein at least one of said first and second nodes is coupled to a node in said first metal.

4. (As Filed) The structure of claim 2, wherein at least one of said first and second nodes is coupled to a node in said second metal.

5. (As Filed) The structure of claim 1, wherein said programmable switch comprises a thin film transistor.

6. (As Filed) The structure of claim 5, wherein at least one of said first and second nodes of said programmable switch further comprises a via structure, said via structure containing a seed metal, said seed metal facilitating a thermally activated phase change of at least one of said thin

film materials to improve conduction of said connect state.

7. (As Filed) The structure of claim 1, wherein said configuration circuit comprises a thin film transistor.

8. (As Filed) The device of claim 1, wherein said configuration circuit comprises a memory element.

9. (As Filed) The structure of claim 8, wherein said memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electro-chemical elements, optical elements and magnetic elements.

10. (Currently Amended) The structure of claim 8, wherein the programmable ~~means~~ switch further comprises:

a pass-gate device, said pass-gate controlled by an output signal from said memory element, said first state generated by an on pass-gate, and said second state generated by an off pass-gate; and

a configuration access to program said memory data, said memory bit polarity generating an on and off control signal to select said state of pass-gate device.

11. (Currently Amended) A wire structure for an integrated circuit having two selectable methods of connecting wires, comprising:

a first selectable method comprising programmable switches, each said switch coupling a wire in a first set to a wire in a second set, and said method providing a means to program a user defined interconnect pattern between said first and second set of wires; and

a second selectable method comprising permanent connections ~~in lieu of said switches~~, each switch in said first selectable method replaced by a connected or a disconnected wire, said permanent connection pattern duplicating one of said user defined interconnect patterns.

12. (As Filed) The structure of claim 11, wherein said programmable switch is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

13. (As Filed) The structure of claim 11, wherein said programmable switch is comprised one of a volatile and a non volatile memory element.

14. (As Filed) The structure of claim 13, wherein said memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electro-chemical elements, optical elements and magnetic elements.

15. (As Filed) The structure of claim 11, wherein said second selectable method further comprises fabricating permanent connections using at least one of a customized metal mask and a customized through-hole mask.

16. (As Filed) The structure of claim 11, wherein said programmable switch further comprises:

one or more connecting devices, each of said devices comprising a connect-state and a disconnect-state, said device coupling a wire in said first set and a wire in said second set; and

a configuration circuit comprising one or more memory elements, each said memory element generating a control signal, said signal comprising a logic-low and a logic-high level, said signal further coupled to one or more of said connecting devices; and

a programmable means of changing data in said memory elements, said change altering said control signal level, said level further altering said connecting device state.

17. (As Filed) The structure of claim 11, said first selectable method is further comprised of:

fabricating an array of programmable cells on a substrate layer; and

fabricating one or more pass-gates on thin-film layers substantially above said substrate layer, each said pass-gate connecting a wire in said first set to a wire in said second set; and

fabricating configuration access transistors and memory elements on said thin-film layers, each said memory element generating a control signal; and

coupling said control signal from each of said thin film memory elements to a gate electrodes of said pass-gates; and

providing programmable access to change said thin film memory data via said thin film access transistors.

18. (As Filed) A semiconductor device for integrated circuits with two selectable

manufacturing configurations, comprising:

a first module layer having an array of structured cells, said module layer having at least one layer of metal; and

a second module layer formed substantially above said first module layer comprising two selectable configurations, wherein:

in a first selectable configuration a programmable interconnect structure is formed to connect said structured cells, and

in a second selectable configuration a customized interconnect structure is formed to connect said structured cells.

19. (As Filed) The device of claim 18, further comprising a third module layer formed substantially above said second module layer comprised of a plurality of metal layers, said metal layers providing conductive wires to complete interconnect and routing of said semiconductor device.

20. (As Filed) The device of claim 18, further comprising:

each said structured cell comprising inputs and outputs, said inputs and outputs formed in said first module layer; and

a portion of said inputs and outputs requiring one of said selectable second modules to connect to each other.

21. (As Filed) The device of claim 18, further comprising:

said first selectable configuration comprised of a plurality of programmable interconnect

patterns, a unique said pattern programmed by a user; and

said second selectable configuration comprised of an interconnect pattern duplicating said unique programmed pattern; and

said array of structured cells comprising an interconnect pattern, said interconnect pattern identical with either of said selectable options.

22. (As Filed) The device of claim 18, wherein said programmable interconnect structure is further comprised of a user configurable memory circuit constructed on a thin film layer comprising one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electro-chemical elements, optical elements and magnetic elements.

23. (Currently Amended) The ~~method~~ device of claim 22, further comprised of said conductive pattern comprising fabricating hard wire controls to replicate a specific memory pattern, wherein replicating comprises:

a logic zero memory output mapped to a hard wire disconnect; and

a logic one memory output mapped to a hard wire connect.